IN THE DRAWINGS:

Please hold in abeyance any requirements for drawing changes pending allowance of the application.

IN THE CLAIMS:

Please cancel claims 8 through 10 without prejudice in accordance with the restriction requirement.

Please add new claims 11 through 14, as shown below, and please amend claims 2 through 4, 6, and 7 as follows.

2. (Amended) The multi-layered circuit structure in accordance with claim 1, wherein said first substrate comprises a signal core, and said second substrate comprises a power core.

3. (Amended) The multi-layered circuit structure in accordance with claim 1, wherein said first substrate comprises a pair of spaced-apart outer signal cores, and said

second substrate comprises an inner power core sandwiched between said pair of spaced-apart outer signal cores.

4. (Amended) The multi-layered circuit structure in accordance with claim 3, wherein said via through holes of said inner power core comprise undercut contact surfaces, and said via through holes of said pair of spaced-apart signal cores have metallic pads that make electrical contact with said undercut contact surfaces of said via through holes of said inner power core.

6. (Amended) The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a signal core, and said second substrate comprises a power core.

7. (Amended) The multi-layered circuit structure in accordance with claim 5, wherein said first substrate comprises a pair of spaced-apart outer signal cores, and said second substrate comprises an inner power core sandwiched between said pair of spaced-apart outer signal cores.

11. (Added) A multi-layered circuit structure, comprising:

first and second spaced-apart substrates, each having conductive via through holes disposed therein; and

a third substrate laminated between said first and second spaced-apart substrates and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first and second spaced-apart substrates, upon lamination of said first and second spaced-apart substrates to said third substrate.

12. (Added) The multi-layered circuit structure in accordance with claim 11, wherein said first and second spaced-apart substrates comprise a signal core, and said third substrate comprises a power core.

13. (Added) The multi-layered circuit structure in accordance with claim 11, wherein said first substrate comprises a pair of spaced-apart outer signal cores, and said